Ref #	Hits	Search Query	DBs	Default Operator	Plurals	Time Stamp
L1	1678	unified adj2 memory uma	US-PGPUB; USPAT	OR	ON	2005/07/07 07:31
L2	139	(tiling tile tiler) adj2 convert$	US-PGPUB; USPAT	OR	ON	2005/07/07 07:49
L3	368038	core adj logic chipset chip adj set bridg$	US-PGPUB; USPAT	OR	ON	2005/07/07 07:36
L4	2	2 same 3	US-PGPUB; USPAT	OR	ON	2005/07/07 07:33
L5	11	2 and 3	US-PGPUB; USPAT	OR	ON	2005/07/07 07:33
L6	9	5 not 4	US-PGPUB; USPAT	OR	ON	2005/07/07 07:34
L7	17090	core adj logic chipset chip adj set	US-PGPUB; USPAT	OR	ON	2005/07/07 07:36
L8	48429	tile tiling tiler	US-PGPUB; USPAT	OR	ON	2005/07/07 07:53
L9	21	7 same 8	US-PGPUB; USPAT	OR	ON	2005/07/07 07:48
L10	1	1 and 9	US-PGPUB; USPAT	OR	ON	2005/07/07 07:36
L11	2	graphic$ same 2	US-PGPUB; USPAT	OR	ON	2005/07/07 07:48
L12	913	(tiling tile tiler) with convert$	US-PGPUB; USPAT	OR	ON	2005/07/07 07:49
L13	13	7 and 12	US-PGPUB; USPAT	OR	ON	2005/07/07 07:50
L14	9	13 not 9	US-PGPUB; USPAT	OR	ON	2005/07/07 07:50
L15	3036	(tile tiling tiler) with (memory storag$ buffer)	US-PGPUB; USPAT	OR	ON	2005/07/07 07:53
L16	213	7 and 15	US-PGPUB; USPAT	OR	ON	2005/07/07 07:53
L17	5	7 same 15	US-PGPUB; USPAT	OR	ON	2005/07/07 07:53

Ref #	Hits	Search Query	DBs	Default Operator	Plurals	Time Stamp
L1	5	tile adj converter	US-PGPUB; USPAT	OR	ON	2005/07/07 09:29
L2	670	linear with tile	US-PGPUB; USPAT	OR	ON	2005/07/07 09:29
L3	67	memory same 2	US-PGPUB; USPAT	OR	ON	2005/07/07 09:30
L4	16	graphic same 3	US-PGPUB; USPAT	OR	ON	2005/07/07 09:41
L5	54	graphic and 3	US-PGPUB; USPAT	OR	ON	2005/07/07 09:30
L6	38	5 not 4	US-PGPUB; USPAT	OR	ON	2005/07/07 09:41